REMARKS

The present amendment is prepared in accordance with the new revised requirements of 37 C.F.R. § 1.121. A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Claims 1, 5 and 19 have been amended to clarify that which applicants regard as the invention.

No new matter has been added.

Rejection under 35 USC § 103

Claims 1, 2, 4, 19, and 20

The Examiner has rejected claims 1, 2, 4, 19, and 20 under 35 U.S.C. 103(a) as being unpatentable over White (U.S. Patent No. 5,535,526) in view of Yan et al. (U.S. Patent No. 6,841,888).

It is submitted that the independent claims, to wit, claims 1, 5 and 19, are directed to methods and electronic modules by attaching a chip to a first surface of a substrate using a first solder interconnection array and attaching a board (e.g., and organic board) to a second surface of the substrate using a second solder interconnection array. In so doing, a space is defined between the board and substrate, whereby this space has a gap height ranging from about 300 microns to about 900 microns with the second solder interconnection array residing entirely within the space.

An essential feature of the invention is that an underfill material is provided within the space after the board has been attached to the substrate but prior to applying compressive forces to the electronic module. The underfill material has a filler material with a particle size ranging from about 32 microns to about 300 microns that is present in an amount ranging from about 60 to 64 weight percent. The underfill material is provided such that it is in direct contact with both the board and the substrate to maintain the space and optimize integrity of the second solder interconnection array during application of compressive forces. The underfill is cured to form a rigid matrix within the space that maintains and enhances the integrity of the second solder interconnection array. Optionally, the underfill material may be applied only at discrete locations within this space.

Applicants disagree with the Examiner's rejection and submit that White is directed to handling/storing chip carriers to prevent amoebas. (Col. 5, ll. 28-30.) It discloses attaching a flip chip to a substrate using solder bumps (steps 102 and 103) followed by flowing encapsulant under the chip to surround all the connections between the chip and the substrate (step 104). (Col. 5, ll. 31-63.) The module is then attached to a circuit board, whereby the formation of amoebas are prevented during reflow heating when mounting the module onto the board by providing a low concentration of free moisture in the encapsulant (step 105), and/or by using lower temperature joining material for module to circuit board joining than for chip to module joining (step 207). (Col. 6, ll. 1-15 and 60-64.) The modules are then stored in air tight bags preferably with desiccant until the time of use to prevent exposure to humidity. (Col. 6, ll. 20-29 and col. 7, ll. 15-18.)

Referring to Fig. 4, applicants disagree with the Examiner's interpretation thereof and submits that White does not disclose or suggest that the space between the substrate 404 and board 416 is provided with an underfill material after the board 416 has been attached to the substrate 404 but prior to applying compressive forces to the electronic module, as is currently claimed. Rather, it is submitted that the underfill material 408 that the Examiner cites resides between the chip 402 and the substrate 404. Applicants submit that nowhere in the White reference is it disclosed, contemplated or suggested to form electronic modules by attaching a chip to a first surface of a substrate using a first solder interconnection array and attaching a board to a second surface of the substrate using a second solder interconnection array to define a space there-between the board and substrate, which is underfilled after the board has been attached to the substrate but prior to applying compressive forces to the electronic module, as is currently claimed.

Also contrary to the Examiner's interpretation, it is submitted that White does not disclose or suggest that the space between the substrate 404 and board 416 has a gap height ranging from about 300 microns to about 900 microns. White discloses that the bonding pads are 5 mil (127 microns) in diameter (not thickness as interpreted by the Examiner) and the spheres of solder are 5 mil (127 microns) in diameter. (Col. 1, ll. 25-30.) White makes no disclosure or suggestion about the height of the pads –any disclosure relating to any dimension of the pads is limited to the diameters of such pads. Further, if one were to speculate about the thickness of the pads of White, referring to the drawings of White, the thickness of the pads are much less than the thickness of the solder bumps which have a 5 mil diameter. As such, it is submitted that the thickness of the pads are nowhere near 5 mils (127 microns) in thickness. As

such, it is submitted that the gap between the substrate 404 and board 416 does not have a gap height ranging from about 300 microns to about 900 microns, as is claimed.

Further in the outstanding Office Action, the Examiner recognizes that White does not expressly teach an underfill with filler and also the filler particle size and composition of the filler, therein citing Yan et al. to overcome this deficiency. The Examiner takes the position that the present invention would have been obvious over White in view of Yan et al. stating that "it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to provide a filler in the underfill used in the process of White as taught by Yan et al."

Applicants disagree and submit that Yan et al. is limited to teaching underfill materials having filler particles with diameters ranging from 1-500 microns. It does not disclose, contemplate or suggest providing such underfill materials between a substrate and board. Further, White does not disclose or contemplate a gap between a board and substrate having a height of about 300 microns to about 900 microns. Again, at most, the gap height between the board and substrate of White is a little more than127 microns (i.e., from the 127 micron diameter of the solder bump), but less than the currently claimed 300 microns.

As such, bearing the foregoing, one skilled in the art at the time of the invention would not have been apprised of the problems associated with large gap heights within the solder interconnections, e.g., those ranging from about 300-900 microns, when examining the White patent, and as such, would not have found a solution to such problem in the Yan et al. patent.

It is for these reasons that applicants submit that claims 1, 2, 4, 19, and 20, and all dependent claims, are not rendered obvious over White in view of Yan et al.

Claims 1, 2, 4, 19, and 20

The Examiner has also rejected claims 1, 2, 4, 19, and 20 under 35 U.S.C. 103(a) as being unpatentable over White in view of Yan et al. and further in view of Matsuda (U.S. Patent No. 6,697,261). The Examiner states that White and Yan et al. do not expressly teach a mechanical support bracket in the assembly; however, cites Matsuda for this deficiency. It is submitted that Matsuda does not disclose, contemplate or suggest a space between a board and substrate having a gap height ranging from about 300 microns to about 900 microns filled with an underfill material having filler particles ranging from about 32 microns to about 300 microns present in an amount ranging from about 60 to 64 weight percent, whereby this underfill material maintains and enhances the integrity of the solder connection between the board and substrate. As such, it is submitted that Matsuda does not overcome the deficiencies of White or Yan et al., alone or in combination.

Claims 5, 7-10, 13, and 14, and 21 and 22

The Examiner has also rejected claims 5, 7-10, 13, 14, 21 and 22 under 35 U.S.C. 103(a) as being unpatentable over White in view of Yan et al. and Morganelli et al. (U.S. Patent No. 7,047,633).

The Examiner recognizes that White and Yan et al. do not expressly teach an underfill material partially encapsulating the second solder interconnection array at discrete locations. Morganelli et al. (US Patent No. 7,047,633) is cited for the limitation of providing a partial underfill material in an interconnection. However, applicants submit that Morganelli does not disclose, contemplate or suggest any of the above-discussed deficiencies of the prior art. In particular, Morganelli does not disclose, contemplate or suggest that an electronic module is formed by attaching a

chip to a first surface of a substrate using a first solder interconnection array and attaching a board to a second surface of the substrate using a second solder interconnection array to define a space there-between that is underfilled after the board has been attached to the substrate but prior to applying compressive forces to the electronic module, as is currently claimed. Also, Morganelli does not disclose or suggest that the space between the board and substrate has a gap height ranging from about 300 microns to about 900 microns, which is filled with the underfill material having filler particles ranging from about 32 microns to about 300 microns present in an amount ranging from about 60 to 64 weight percent.

As such, it is submitted that Morganelli et al. does not overcome the deficiencies of White or Yan et al., alone or in combination.

Claim 6

The Examiner has further rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over White in view of Yan et al. and Morganelli et al. as applied to claim 5 above, and further in view of Baba et al. (U.S. Patent No. 6,582,993).

The Examiner recognizes that White, Yan et al. and Morganelli et al. do not expressly teach cleaning the organic board or substrate prior to depositing the underfill, and cites Baba et al.to overcome this deficiency. Applicants disagree with the rejection of claim 6 and continue to submit that claim 1, from which claim 6 depends, is not obvious over the combination of White, Yan et al. and Morganelli et al. for the reasons discussed in detail above. It is submitted that Morganelli et al. does not overcome these deficiencies since it does not dislcose or suggest a space between a board and substrate having a gap height ranging from about 300 microns to about 900 microns filled with an underfill material having filler particles ranging from about 32 microns to

about 300 microns present in an amount ranging from about 60 to 64 weight percent, whereby this underfill material maintains and enhances the integrity of the solder connection between the board and substrate.

Applicant submits that claim 6 is not obvious over White, Yan et al. and Morganelli et al., or Baba et al, alone or in any proper combination thereof.

Claims 15-18

The Examiner has further rejected claims 15-18 under 35 U.S.C. 103(a) as being unpatentable over White in view of Yan et al. and Morganelli et al. as applied to claim 5 above and further in view of Kumamoto et al. (U.S. Patent No. 6,632,704). The Examiner continues to cite Kumamoto stating that although the thixotropic index range is not mentioned by Kumamoto et al., the numbers in table 1 of Kumamoto et al. closely match the corresponding numbers claimed by applicant. This is not a basis of a supported prima case of obviousness.

Applicants continue to submit that the disclosed amount of filler material (i.e., filler material present in an amount ranging from about 80% by weight per solution) in Kumamoto et al. is a difference in kind, not degree. It is for this reason, and the fact that Kumamoto et al. does not disclose, contemplate or suggest any of the above discussed deficiencies of the prior art,that applicants submit that Kumamoto et al. does not overcome the deficiencies of White, Yan et al. nor Morganelli et al., alone or in any proper combination thereof.

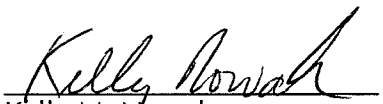
It is again submitted that the suggestion to make the claimed structure, carry out the claimed process and the reasonable expectation of success there-from must be founded in the prior art, not in Applicant's disclosure. *In re Vaech* (CAFC 1991) 20 USPQ2d 1438. The cited reference, and not in retrospect, must suggest doing what

Applicants have done. *In re Skoll* (CCPA 1975) 187 USPQ 481. Applicants submit that the cited references, alone or in combination, do not suggest doing what applicants have done, such that applicants' invention would only be found based on applicants' own disclosure, which of course is improper as a hindsight reconstruction of applicants' invention. *Id., W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983) (Hindsight based on reading of the patent in issue may not be used to aid in determining obviousness). Likewise, hindsight and the level of ordinary skill in the art may not be used to supply a component missing from the cited references. *Al-Site Corp. v. VSI International, Inc.*, 174 F.3d 1308, 1324, 50 USPQ2d 1161, 1171 (Fed. Cir. 1999).

In view of the foregoing, and under the applicable patent law in this area, it is respectfully submitted that the claims are properly allowable under 35 USC 103.

It is respectfully submitted that the application has now been brought into a condition where allowance of the case is proper. Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,



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